AN-277

Application Note
Integrated Circuits

OVERSHOOT AND RINGING IN HIGH SPEED DIGITAL SYSTEMS

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The amount of overshoot and ringing that may be expected in a system is determined as a function of driving source impedance, rise time, wiring length, and loading. Determination of allowed overshoot and methods of reducing overshoot are discussed for conventional point to point wiring methods. Capacitive loading effects of MECL devices and circuit hardware are also discussed.

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OVERSHOOT AND RINGING IN HIGH SPEED DIGITAL SYSTEMS

Whenever a switching circuit with low output impedance and fast risetime is used to drive a signal lead that is connected to several gates, overshoot will be present. The term overshoot, as used in this note, is defined as the peak to peak voltage difference between the most positive portion of the rising edge of a waveform and the "1" logic level of the waveform after all transients have decayed. In general, the lower the output impedance of a gate, the faster the risetime, the longer the wiring length, and the larger the fanout, the greater the overshoot caused when switching occurs. This note contains several tables and sets of photographs illustrating the overshoot that can be expected under various worst case configurations and loadings. Methods of overshoot reduction are applied with tabulated results from which general conclusions and guidelines are drawn.

The exact simulation of an integrated circuit load or the loading of several devices is extremely difficult with passive components. This is due to the complex and non-linear input impedance of a MECL device. The input capacitance goes through a peak value of approximately 15pF during a logic transition and averages out to less than 5pF over the entire logic swing. The input resistance will be about 50KΩ (worst case) at a logic "1" level. The input resistance will decrease exponentially if saturation of the MECL input is approached. (A MECL gate may be driven into saturation by sufficient overshoot on the input waveform, especially at high temperatures.) For system design purposes a worst case input capacitance of 5pF per device input and a 50k resistance to V_{EE} may be utilized. If sockets for the gates are used, an additional 1pF should be added per gate input. Wiring capacitance using teflon coated wire is about 1 pF per inch. Inductance per unit length of wire is about 0.02 μH per inch. These values will vary by a large amount depending upon "lead dress" and, therefore, should be considered only as "ball park" figures. When circuit measurements are being made, oscilloscope probe capacitance should be considered. The capacitance of a probe will vary from 1.8pF to about 10pF depending upon the probe design.

Attempts were made to simulate the loading caused by various fan-outs with discrete components. The best simulation was obtained by the following circuit, Figure 1, which will help to explain the parameters affecting overshoot. R_O stands for the output incremental resistance of the gate used as a driver. Values are approximately: MC301--20Ω, MC365--12Ω, MC369--5Ω. L is the series inductance of the signal lead and R_I is the input resistance of the gates used as the load. C is the shunt capacitance caused by the fan-out, wiring capacitance, socket capacitance, and probe capacitance. The value of C is 8-10pF per fan-out. R_D is necessary to damp out excessive overshoot which is caused by the lumped value of C. C is chosen to give rise time equivalent to the measured value for the given fan-out. R_D is on the order of 20Ω with higher values for small fan-out and smaller values for large fan-outs.

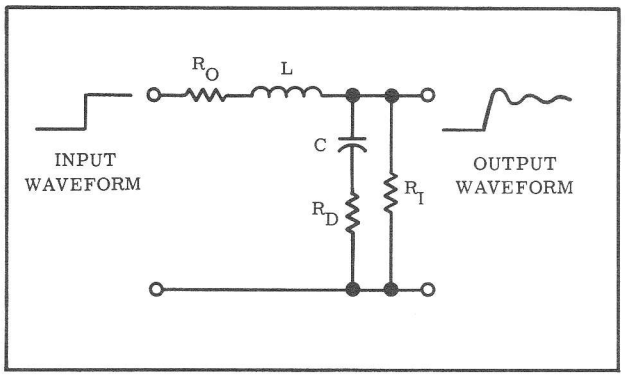


FIGURE 1 — APPROXIMATE EQUIVALENT CIRCUIT

This load only simulates overshoot and rise time as can be seen by comparing photographs 2, 8, and 14 with 5, 11, and 17 respectively. The period of oscillation is longer for the simulated load, indicating that the value of C is higher than with the actual load. The effective capacitance of the actual load may be shown to be about 6-7pF per fan-out, i.e. 2-3pF less than in the simulated load. The difference in period of oscillation and damping indicates just how approximate the simulated load is.

How much overshoot can occur under worst case conditions in a MECL system? This question is answered by the data which are shown in the following tables. These data were obtained by using the MC301, MC365, and MC369 gates as drivers. MC356's and MC364's were used as fan-out devices. Detailed information may be found on MECL devices in Designer's Data Brochures DS9046-R1 and DS9044, and AN244. Lead lengths of 3", 6" and 12" were used with the loads constructed on printed circuit boards and plugged into a single socket which terminated the particular lead. This simulates a worst case situation since fan-out is not usually lumped at the end of a single lead. The devices used as drivers were picked at random and other devices may give somewhat different results due to output impedance and output risetime.

How much overshoot can be tolerated in a MECL system? This question is relatively easy to answer in the case of driving flip-flops, but becomes more difficult when referring to gates. When driving flip-flops, one $\overline{J}$ input may be clocked and the other inhibited at a worst case "1" level. If the level of the clocked J input exceeds the inhibiting level on the other J input by more than the required amplitude to toggle a sensitive flip-flop, then false information may be passed into the flip-flop. For room temperature operation, overshoot should

DRIVER GATE	FAN-OUT	3" LEAD LENGTH		6" LEAD LENGTH		12" LEAD LENGTH	
		OS	RT	OS	RT	OS	RT
MC301	2-MC356	5mV	8.9ns	10mV	7.7ns	50mV	6.8ns
MC301	5-MC356	40mV	9.2ns	60mV	8.5ns	110mV	8.0ns
MC301	10-MC356	90mV	10.9ns	115mV	10.9ns	175mV	11.1ns
MC301	15-MC356	95mV	12.1ns	135mV	12.0ns	200mV	12.3ns
MC365	2-MC356	40mV	6.7ns	70mV	6.2ns	145mV	5.4ns
MC365	5-MC356	80mV	6.9ns	140mV	6.6ns	215mV	6.6ns
MC365	10-MC356	150mV	8.2ns	205mV	8.2ns	270mV	8.4ns
MC365	15-MC356	180mV	9.0ns	220mV	10.0ns	300mV	10.3ns
MC369	2-MC356	80mV	4.2ns	200mV	4.5ns	300mV	4.4ns
MC369	5-MC356	120mV	5.2ns	220mV	5.5ns	330mV	6.3ns
MC369	10-MC356	180mV	7.4ns	220mV	7.7ns	350mV	9.1ns
MC369	15-MC356	200mV	8.9ns	270mV	9.0ns	370mV	9.9ns

TABLE 1 — MEASURED OVERSHOOT AND RISE TIME MC356 AS LOAD

DRIVER GATE	J-K COMMON FAN-OUT	3" LEAD LENGTH		6" LEAD LENGTH		12" LEAD LENGTH	
		OS	RT	OS	RT	OS	RT
MC301	1-MC364	0mV	7.5ns	0mV	7.8ns	0mV	6.0ns
MC301	2-MC364	45mV	7.5ns	70mV	7.3ns	135mV	7.2ns
MC301	5-MC364	85mV	8.6ns	130mV	8.8ns	200mV	8.8ns
MC301	10-MC364	160mV	12.9ns	190mV	13.0ns	270mV	13.5ns
MC365	1-MC364	0mV	6.7ns	0mV	4.7ns	55mV	4.8ns
MC365	2-MC364	100mV	5.9ns	165mV	5.8ns	250mV	6.0ns
MC365	5-MC364	160mV	6.7ns	210mV	6.9ns	340mV	7.3ns
MC365	10-MC364	180mV	9.9ns	230mV	11.3ns	370mV	11.5ns
MC369	1-MC364	0mV	4.5ns	50mV	4.1ns	280mV	4.1ns
MC369	2-MC364	180mV	4.9ns	280mV	5.0ns	350mV	5.4ns
MC369	5-MC364	250mV	6.0ns	340mV	6.4ns	420mV	6.4ns
MC369	10-MC364	250mV	8.8ns	340mV	9.3ns	440mV	10.1ns

TABLE 2 — MEASURED OVERSHOOT AND RISE TIME MC364 (CLOCKED) AS LOAD

be less than 150 mV. For worst case design over the full temperature range (-55°C to +125°C), overshoot should be limited to 100 mV or less. Although a regular gate will tolerate far more overshoot than the above-mentioned values, the worst case value of 100 mV should be used in system design. If high overshoot levels occur in a system, problems caused by the cross-coupling of noise from one signal lead to another will be compounded. For example, if 200 mV of overshoot is allowed, a normal transition of 800 mV would be changed to a 1V transition, therefore increasing cross-coupling of noise by 25%.

It is obvious that the worst case values of overshoot shown in Tables 1 and 2 are excessive. How then can overshoot be reduced? It can be seen from the approximate equivalent circuit, Figure 1, that overshoot and the associated ringing is caused primarily by the values of L and C which dominate the other parameters for large fan-outs. Overshoot may be reduced by decreasing L and C and/or adding to the damping by increasing R_O or R_D. The value of L may be decreased by running the lead close to a ground plane or using a flat conductor that has less inductance per unit length. Figures 3, 9, and 15 compared with 4, 10, and 16 respectively, show the striking difference in overshoot for 12" of teflon coated wire driving a fan-out of 15 gates when the wire is touching the ground plane and when it is an average of 3" above the ground plane. The value of C is difficult to reduce. The equivalent capacitance per gate input may be varied by perhaps 2pF depending upon the use of sockets or the direct wiring of the integrated circuits, and the method of wiring used.

The most effective method of reducing overshoot is the reduction of $L\frac{di}{dt}$, the voltage drop across L due to the rate of change of current. One way to accomplish this is by decreasing lead length or running multiple wires between the driver and load. This method is often not practical. The insertion of a resistor in series with the lead, thus increasing the series damping resistance, is the most effective method of overshoot reduction. The time constant of the transmission path is then increased, therefore causing a trade-off with risetime. The addition of a resistor causes a DC voltage drop and large values must be avoided to prevent "1" level degradation. Table 3 gives the maximum value of series resistance that may be inserted for worst case design for a given fan-out and driver.

Since capacitively coupled flip-flops toggle on peak-to-peak amplitude and are relatively unaffected by voltage input levels, higher values of series resistance may be

LOADING		MAXIMUM SERIES RESISTANCE (R_S)		
DC FAN-OUT	MAXIMUM EQUIVALENT LOAD CURRENT	STANDARD GATE DRIVER R_O=22	LINE DRIVER MC315/MC365 R_O=15	CLOCK DRIVER MC369 R_O=5
25	2.5mA	0	7	17
15	1.5mA	14	21	31
10	1.0mA	33	40	50
5	0.5mA	88	95	105
3	0.3mA	160	170	180
2	0.2mA	250	260	270
1	0.1mA	530	535	545

NOTE: Worst Case values are calculated from $R_O + R_S = \frac{\Delta V}{\Delta I}$

ΔV = 55mV maximum allowed "1" level voltage change (no load to full load)

ΔI = change in load current (no load to full load) for given fan-out

R_O = incremental output resistance of driver gate

R_S = series resistance added in lead between driver and fan-out

TABLE 3 — MAXIMUM ALLOWED VALUES OF SERIES RESISTANCE VS. FAN-OUT

employed. The limit on the values of resistance is determined by the worst case amplitude vs. risetime curves which may be found in AN244. The added resistance, if relatively large in value, forms an R-C integration network which determines the risetime. This may be observed in Table 4.

It is seen from Table 4 that the values of required series resistance become marginal for high fan-outs with 12" signal leads when compared to the allowed values shown in Table 3. Therefore, when driving a high fan-out with fast risetime it may be more desirable to use the following method: A separate signal lead and series resistor from the driver to each fan-out is utilized. This method may be used for a fan-out of 20 clocked flip-flops using the MC369 as a driver. The risetime to each flip-flop or gate is appreciably less for this method than when driving the devices with a single signal lead and resistor. Refer to AN244 for a table listing the required values of resistance for various fan-outs.

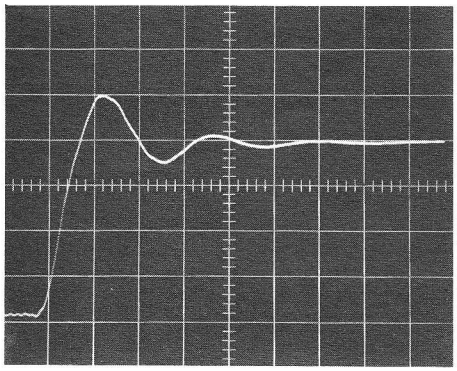
Another method of reducing overshoot is the addition of a ferrite bead around the signal lead between the driver and the load. This is another method of trading overshoot for risetime. Advantages of the ferrite bead are low cost and no shift produced in DC levels. Disadvantages are that it is effective for only small fan-outs, fast risetimes, and long lead lengths. The ferrite bead adds inductance to the signal lead at low frequencies, but this is an inductance of very low Q at high frequencies. Therefore, attenuation is produced for the high frequency components of the risetime, resulting in a slower risetime as seen by the load. Once the risetime is reduced to about 12ns, the addition of further ferrite beads to the signal line will not appreciably reduce overshoot and may actually increase overshoot for slower risetimes.

The following photographs will serve to illustrate the data shown previously. All photographs are taken with the following constants: Horizontal deflection rate 1cm per 20ns, Vertical deflection 1cm per 200mV, and signal lead lengths of 12 inches. The following notation is used for the photographs. OS = overshoot, tr = risetime, and W = 1/8", W = 0", W = 3" which stand for wire 1/8" above ground plane, 0" above ground plane and 3" above ground plane respectively. L stands for load with "A" being the actual integrated load and "S" being the simulated load. R_S is the value of series resistance inserted in the signal lead. The simulated load used in Figures 5, 7, 11, 13 was C = 150pF, R_D = 15Ω, R_I = 3K (refer to Figure 1), while the simulated load in Figures 17, 19 was C = 160pF, R_D = 8 , R_I = 3K.

DRIVER GATE	FAN-OUT	R	3" LEAD LENGTH OVERSHOOT	3" LEAD LENGTH RISETIME	R	6" LEAD LENGTH OVERSHOOT	6" LEAD LENGTH RISETIME	R	12" LEAD LENGTH OVERSHOOT	12" LEAD LENGTH RISETIME
MC301	10-MC356	0	90mV	10.9ns	5	100mV	11.7ns	18	95mV	12.8ns
MC301	15-MC356	0	95mV	12.1ns	12	90mV	14.3ns	12	95mV	14.4ns
MC301	5-MC364	0	85mV	8.6ns	13	90mV	9.9ns	27	100mV	10.2ns
MC301	10-MC364	10	95mV	14.2ns	13	100mV	14.6ns	24	95mV	15.9ns
MC365	10-MC356	10	90mV	9.4ns	15	95mV	9.8ns	25	95mV	10.3ns
MC365	15-MC356	10	100mV	10.3ns	15	100mV	10.9ns	24	95mV	11.8ns
MC365	5-MC364	20	95mV	8.5ns	27	100mV	8.7ns	51	90mV	9.8ns
MC365	10-MC364	13	95mV	11.9ns	18	95mV	12.6ns	27	95mV	13.8ns
MC369	2-MC356	0	80mV	5.1ns	24	90mV	5.4ns	62	100mV	6.0ns
MC369	5-MC356	5	100mV	5.9ns	24	100mV	6.8ns	43	100mV	7.6ns
MC369	10-MC356	10	100mV	8.7ns	24	90mV	10.5ns	33	90mV	11.4ns
MC369	15-MC356	10	95mV	10.2ns	18	95mV	11.4ns	27	95mV	12.7ns
MC369	1-MC364	0	0	4.8ns	0	50mV	3.9ns	68	90mV	4.0ns
MC369	2-MC364	27	100mV	5.9ns	62	95mV	6.7ns	75	100mV	6.8ns
MC369	5-MC364	22	90mV	7.5ns	39	100mV	8.2ns	47	100mV	8.6ns
MC369	10-MC364	15	90mV	10.9ns	22	100mV	11.9ns	33	100mV	13.4ns

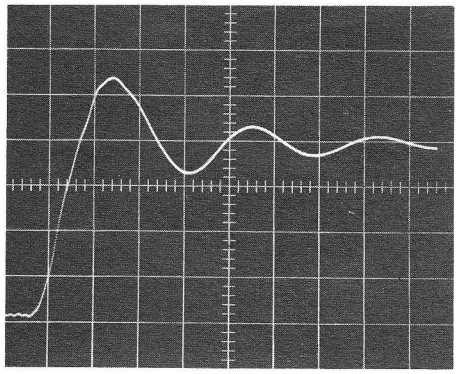
TABLE 4 — REQUIRED SERIES RESISTANCE TO REDUCE OVERSHOOT TO AN ACCEPTABLE LEVEL

THE FOLLOWING SIX PHOTOGRAPHS ARE FOR DRIVER = MC301 FAN-OUT = 15 MC356'S



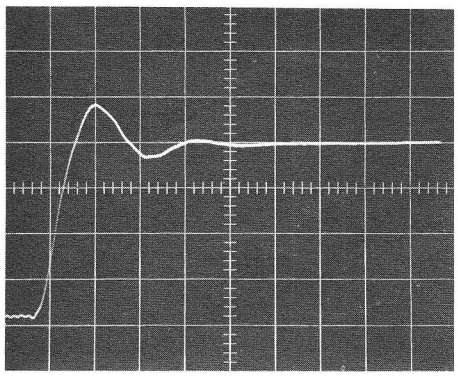
t_r = 12.3ns
w = 1/8"
R_S = 0Ω
OS = 200mV
L = A

FIGURE 2



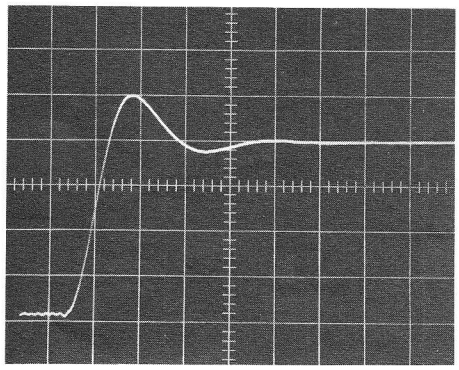
t_r = 14.2ns
w = 3"
R_S = 0Ω
OS = 280mV
L = A

FIGURE 3



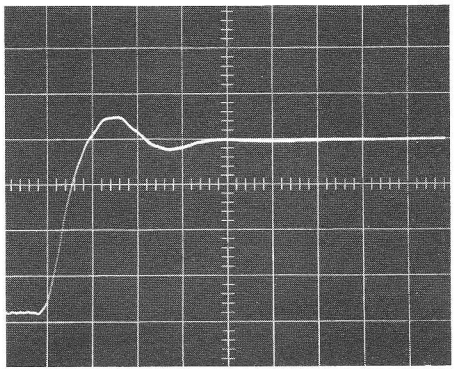
t_r = 12.3ns
w = 0"
R_S = 0Ω
OS = 175mV
L = A

FIGURE 4



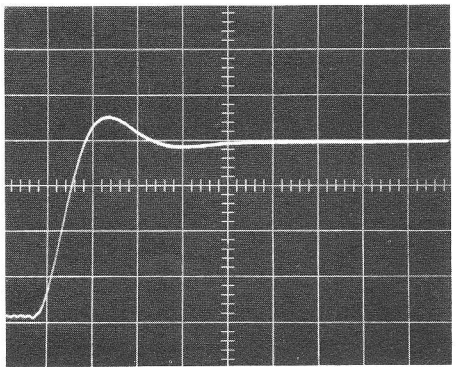
t_r = 12.8ns
w = 1/8"
R_S = 0Ω
OS = 200mV
L = S

FIGURE 5



t_r = 14.7ns
w = 1/8"
R_S = 15Ω
OS = 95mV
L = A

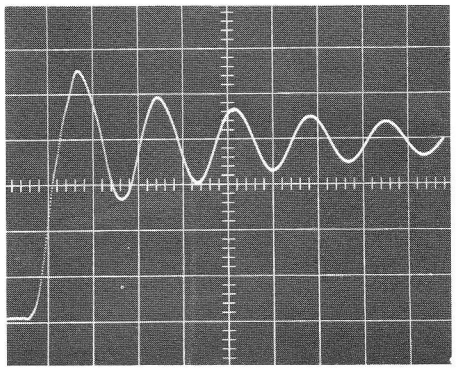
FIGURE 6



t_r = 15.3ns
w = 1/8"
R_S = 15Ω
OS = 100mV
L = S

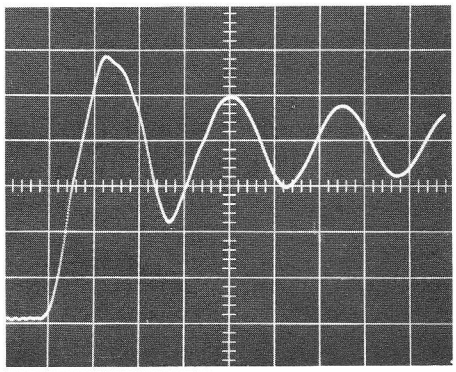
FIGURE 7

THE FOLLOWING SIX PHOTOGRAPHS ARE FOR DRIVER = MC365
FAN-OUT = 15 MC356'S



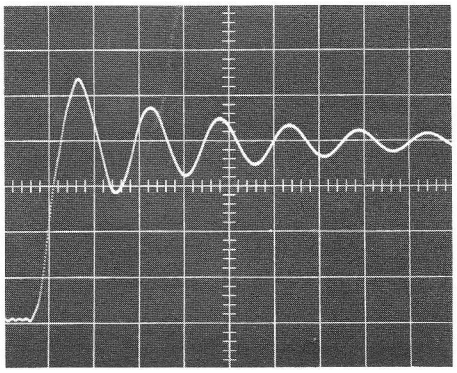
t_r = 10.2ns
w = 1/8"
R_S = 0
OS = 300mV
L = A

FIGURE 8



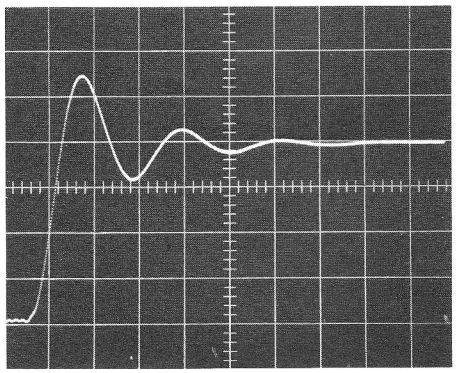
t_r = 12.9ns
w = 3"
R_S = 0
OS = 360mV
L = A

FIGURE 9



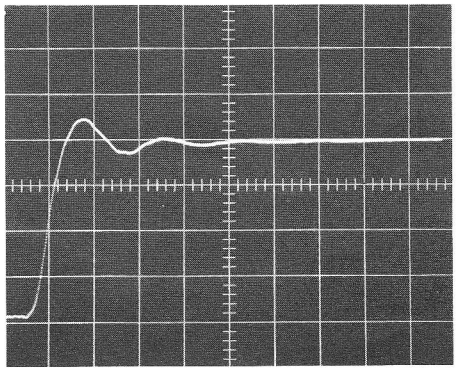
t_r = 9.5ns
w = 0"
R_S = 0
OS = 280mV
L = A

FIGURE 10



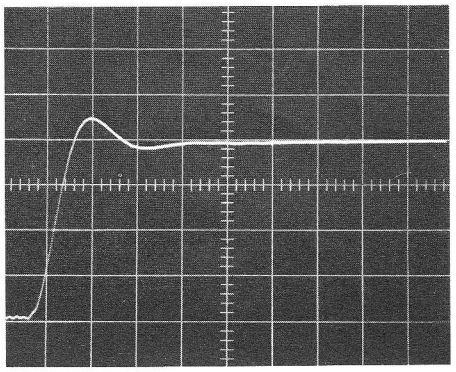
t_r = 10.2ns
w = 1/8"
R_S = 0
OS = 300mV
L = S

FIGURE 11



t_r = 11.8ns
w = 1/8"
R_S = 24Ω
OS = 100mV
L = A

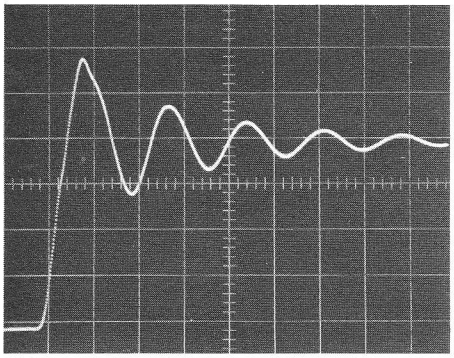
FIGURE 12



t_r = 13.0ns
w = 1/8"
R_S = 24Ω
OS = 100mV
L = S

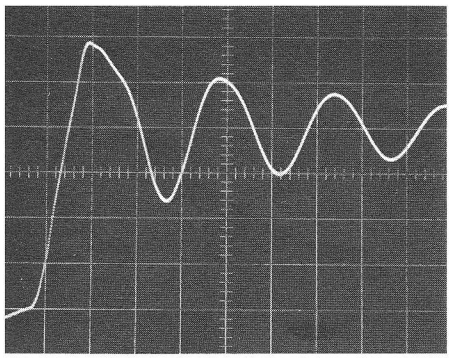
FIGURE 13

THE FOLLOWING SIX PHOTOGRAPHS ARE FOR DRIVER = MC369
FAN-OUT = 15 MC356'S



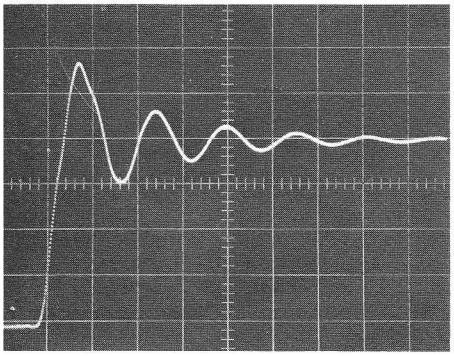
t_r = 8.8ns
w = 1/8"
R_S = 0
OS = 370mV
L = A

FIGURE 14



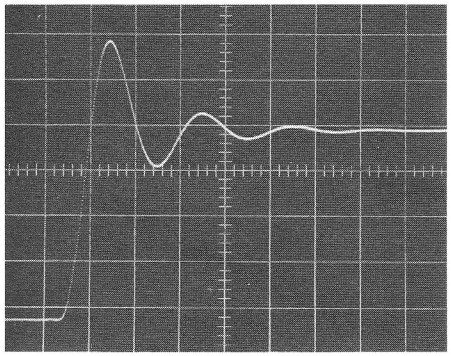
t_r = 12.0ns
w = 3"
R_S = 0
OS = 390mV
L = A

FIGURE 15



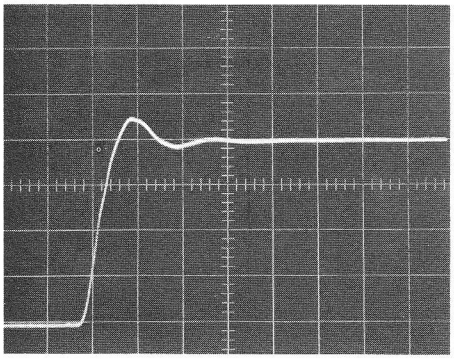
t_r = 8.3ns
w = 0"
R_S = 0
OS = 360mV
L = A

FIGURE 16



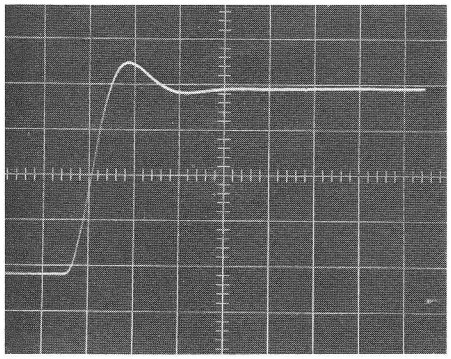
t_r = 9.2ns
w = 1/8"
R_S = 0
OS = 380mV
L = S

FIGURE 17



t_r = 11.6ns
w = 1/8"
R_S = 27Ω
OS = 100mV
L = A

FIGURE 18



t_r = 13.4ns
w = 1/8"
R_S = 27Ω
OS = 100mV
L = S

FIGURE 19

CONCLUSIONS

It has been shown that overshoot can be a system problem for long lead lengths and "lumped" fan-outs and that the amount of overshoot is primarily determined by system layout and geometries. Overshoot to typical fan-outs may be reduced to acceptable levels by inserting resistance of the proper value in series with the driver output lead. Higher fan-outs may be driven with fast risetimes by inserting a resistor of appropriate value in series with the input to each integrated circuit load, and running a separate lead from the driver to each resistor. Also, ferrite beads may be used to advantage for certain configurations of long leads and relatively low fan-outs.

As system speeds increase and MECL gates with risetimes of 2ns or less are utilized, these methods will not be useful for reducing overshoot. Strip line techniques utilizing multi-layer printed circuit boards, controlled line impedance, and terminated transmission lines will solve overshoot problems for logic into the sub-nanosecond region.

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